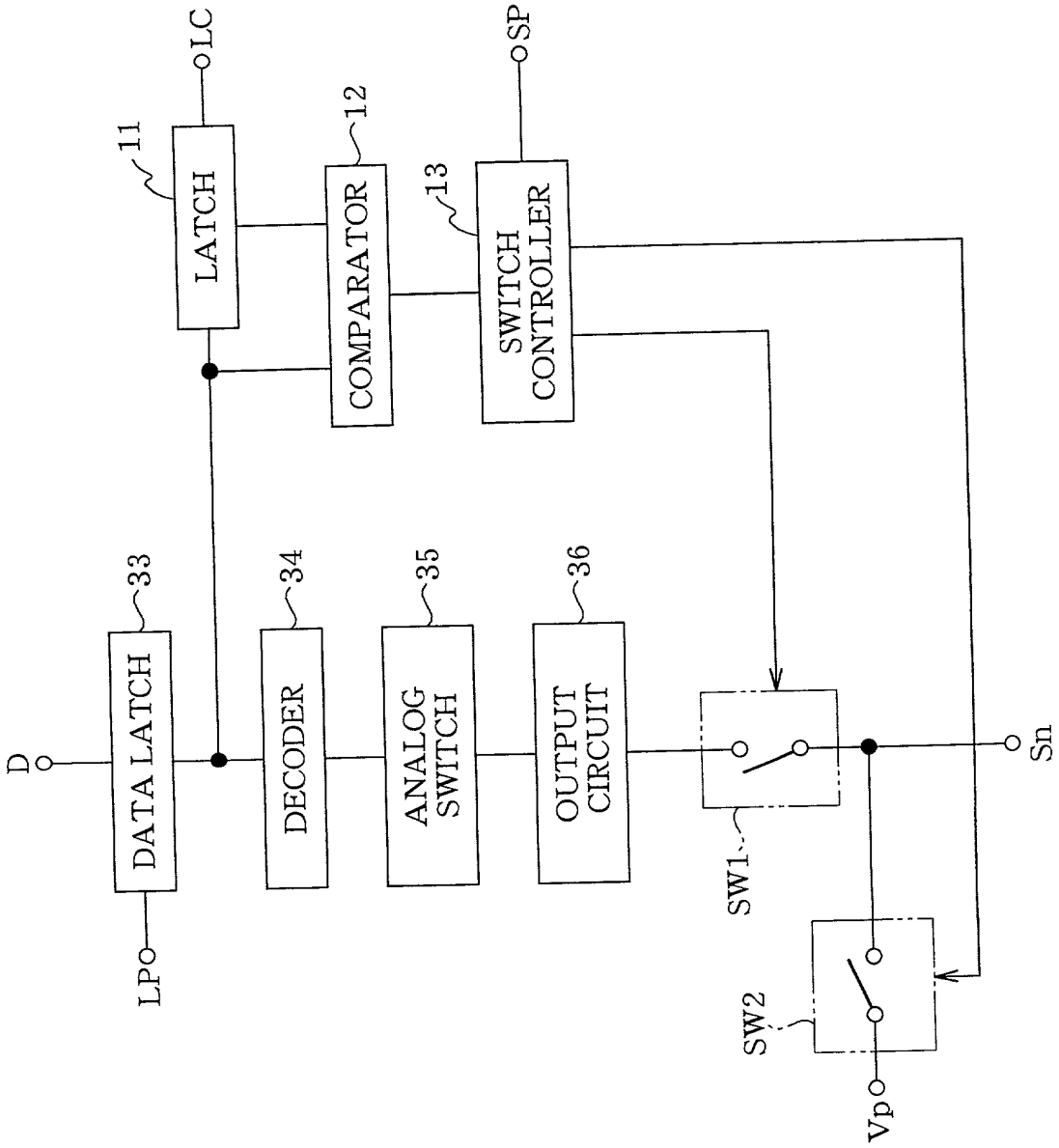

D
LP
DATA LATCH
33
LATCH
11
LC
DECODER
34
COMPARATOR
12
ANALOG SWITCH
35
SWITCH CONTROLLER
13
SP
OUTPUT CIRCUIT
36
SW1
SW2
Vp
Sn

FIG. 1

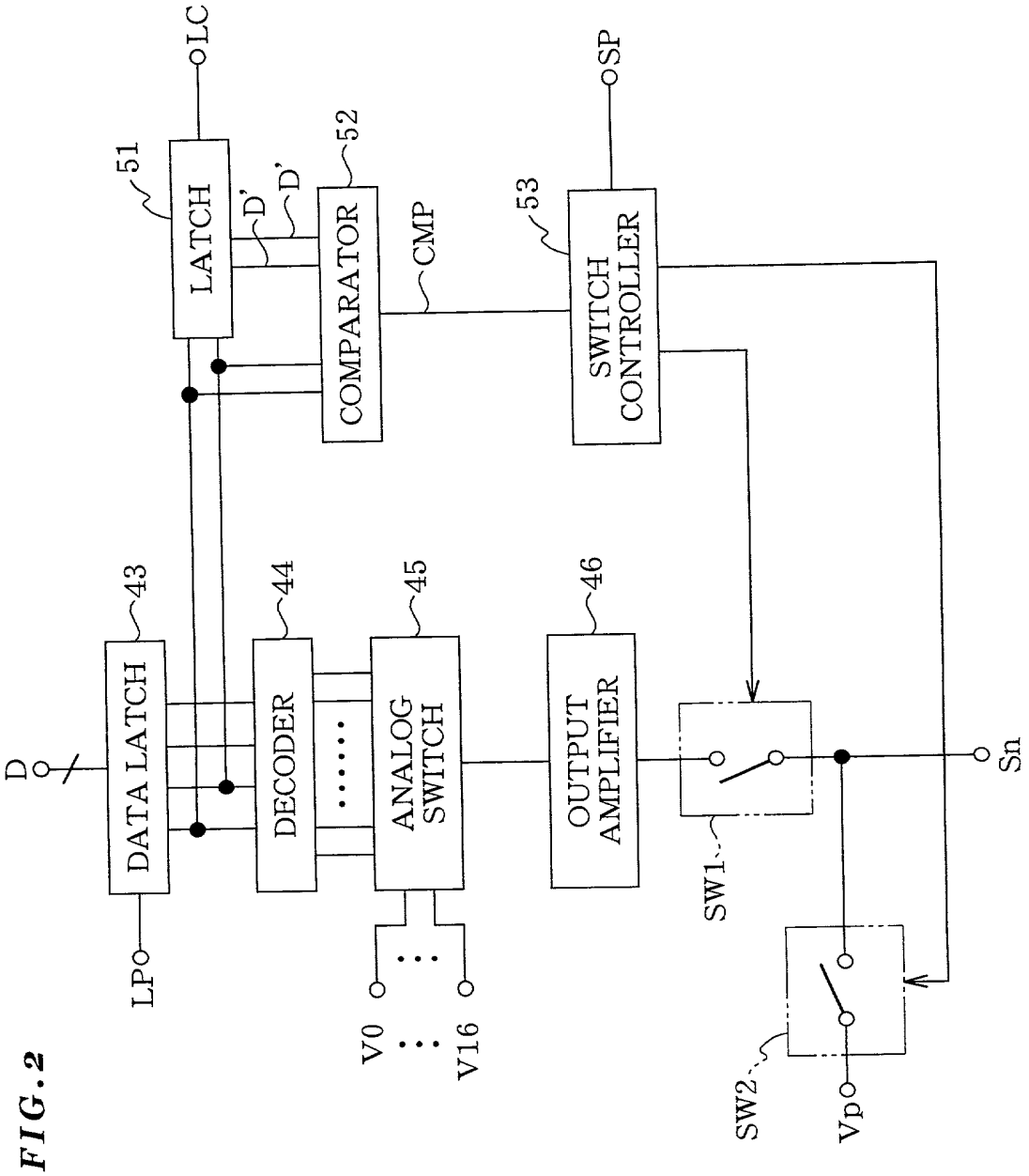
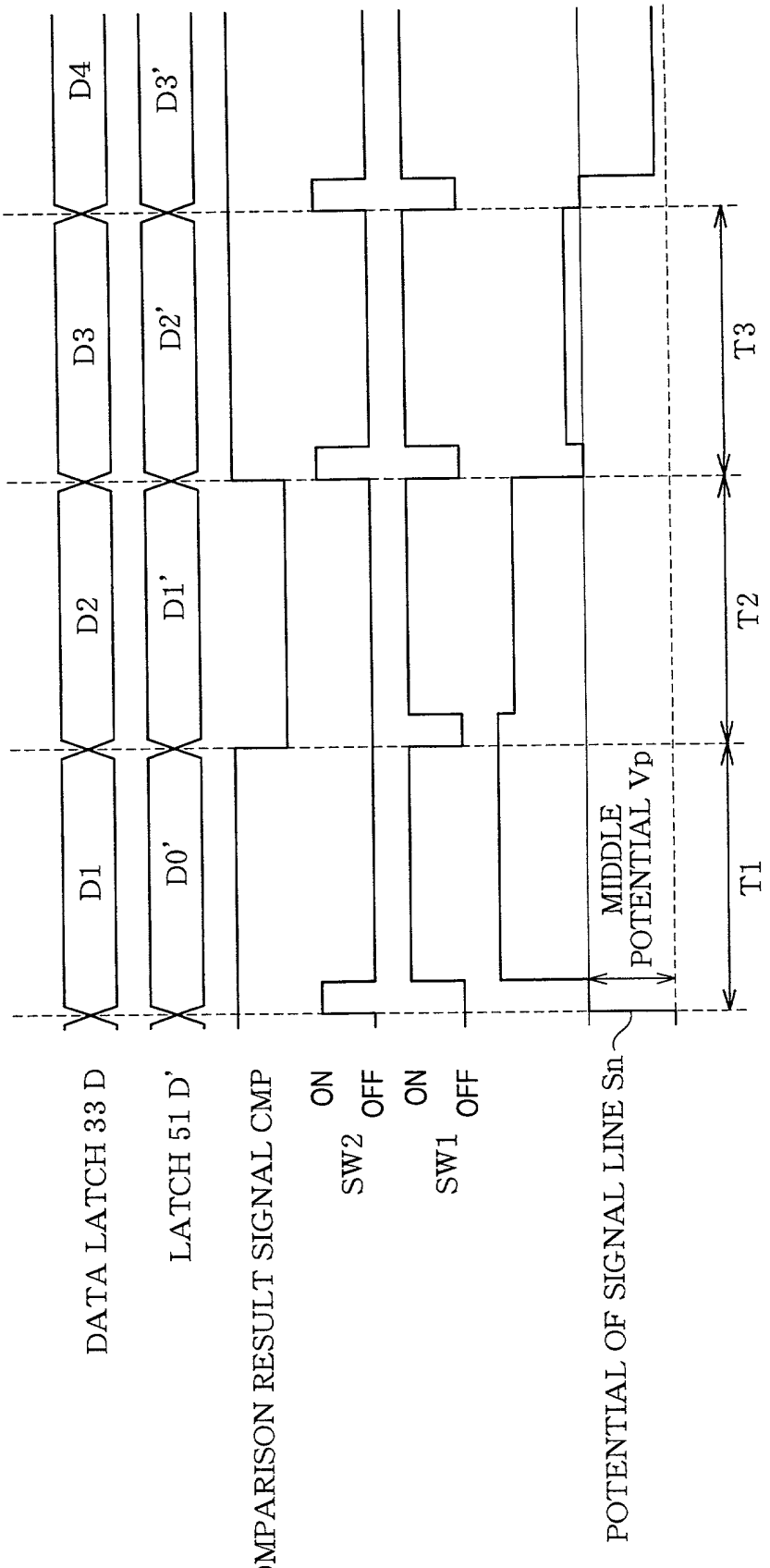

D
DATA LATCH
43
LP
LATCH
51
LC
D'
D'
COMPARATOR
52
CMP
DECODER
44
ANALOG SWITCH
45
V0
V16
OUTPUT AMPLIFIER
46
SWITCH CONTROLLER
53
SP
SW1
SW2
Vp
Sn

FIG. 2

FIG. 3


DATA LATCH 33 D
LATCH 51 D'
COMPARISON RESULT SIGNAL CMP
SW2
ON
OFF
SW1
ON
OFF
POTENTIAL OF SIGNAL LINE Sn
MIDDLE POTENTIAL Vp
D1
D2
D3
D4
D0'
D1'
D2'
D3'
T1
T2
T3

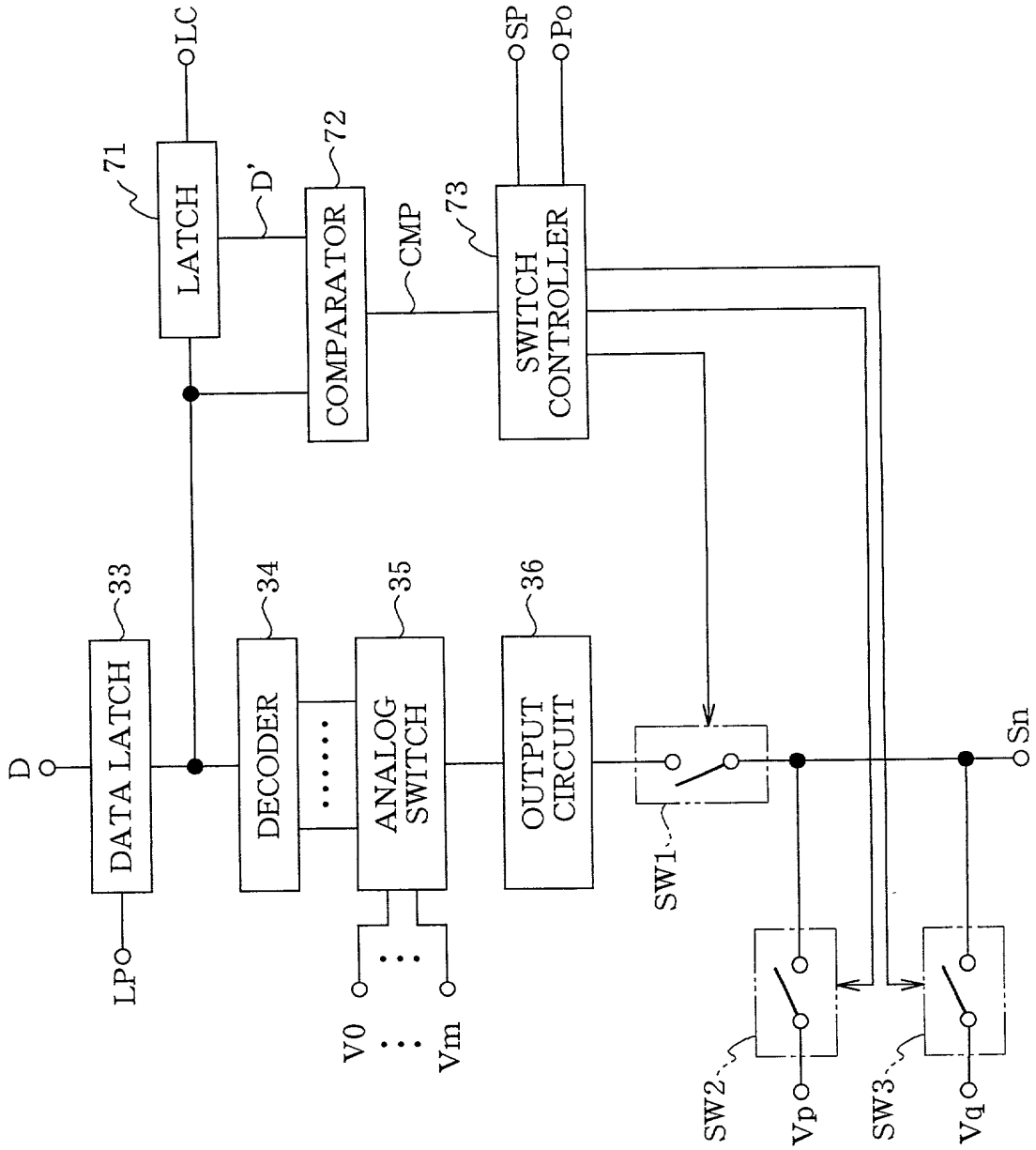
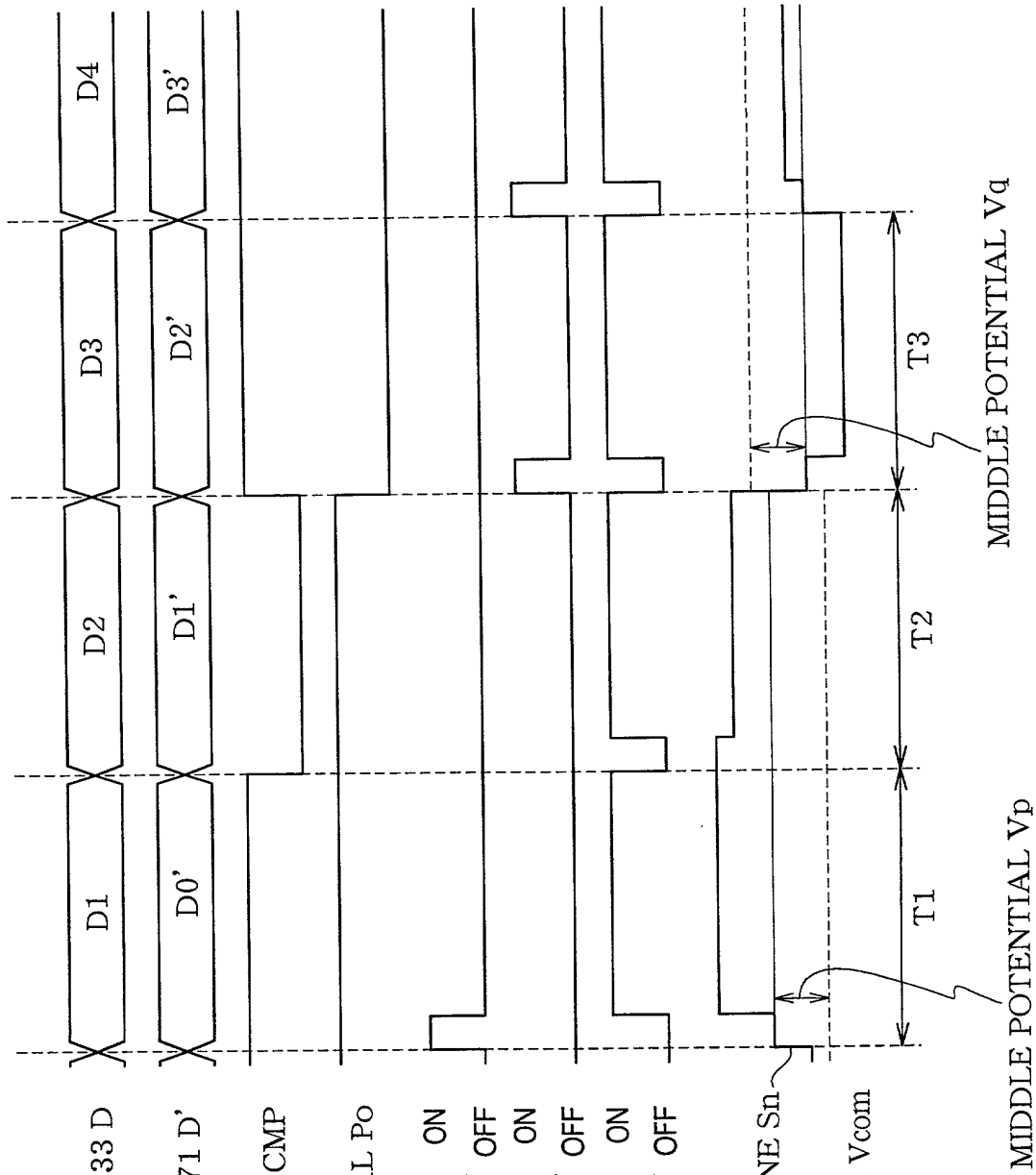

D
DATA LATCH
33
LP
DECODER
34
ANALOG SWITCH
35
V0
Vm
OUTPUT CIRCUIT
36
SW1
Sn
SW2
Vp
SW3
Vq
LATCH
71
LC
D'
COMPARATOR
72
CMP
SWITCH CONTROLLER
73
SP
Po

FIG. 4

FIG. 5


DATA LATCH 33 D
LATCH 71 D'
COMPARISON RESULT SIGNAL CMP
POLARITY INVERSION SIGNAL Po
SW2
SW3
SW1
ON
OFF
POTENTIAL OF SIGNAL LINE Sn
COMMON POTENTIAL Vcom
D1
D2
D3
D4
D0'
D1'
D2'
D3'
T1
T2
T3
MIDDLE POTENTIAL Vp
MIDDLE POTENTIAL Vq

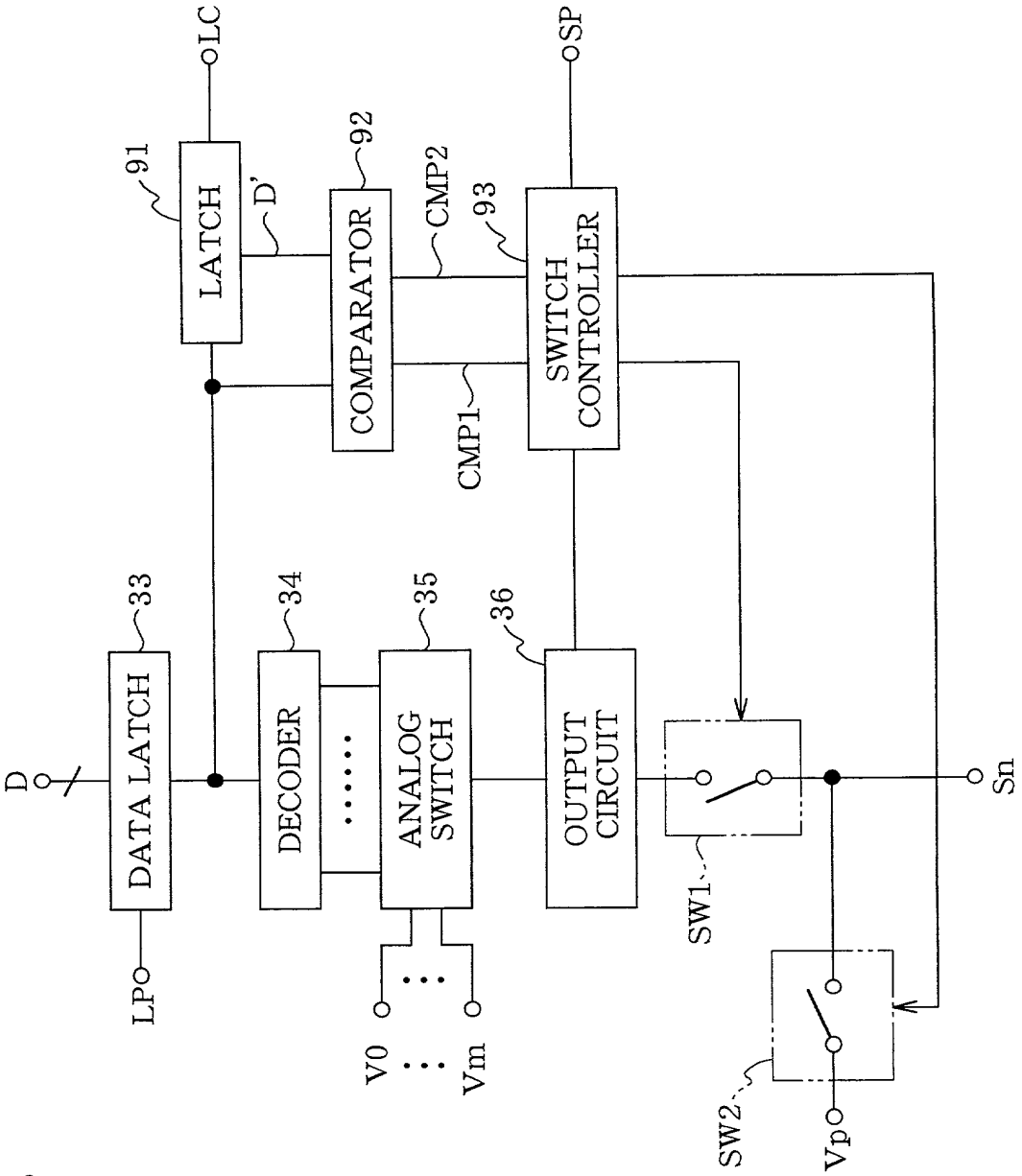

D
DATA LATCH
33
LP
LATCH
91
LC
D'
COMPARATOR
92
CMP2
93
CMP1
SWITCH CONTROLLER
SP
DECODER
34
ANALOG SWITCH
35
V0
Vm
OUTPUT CIRCUIT
36
SW1
SW2
Vp
Sn

FIG. 6

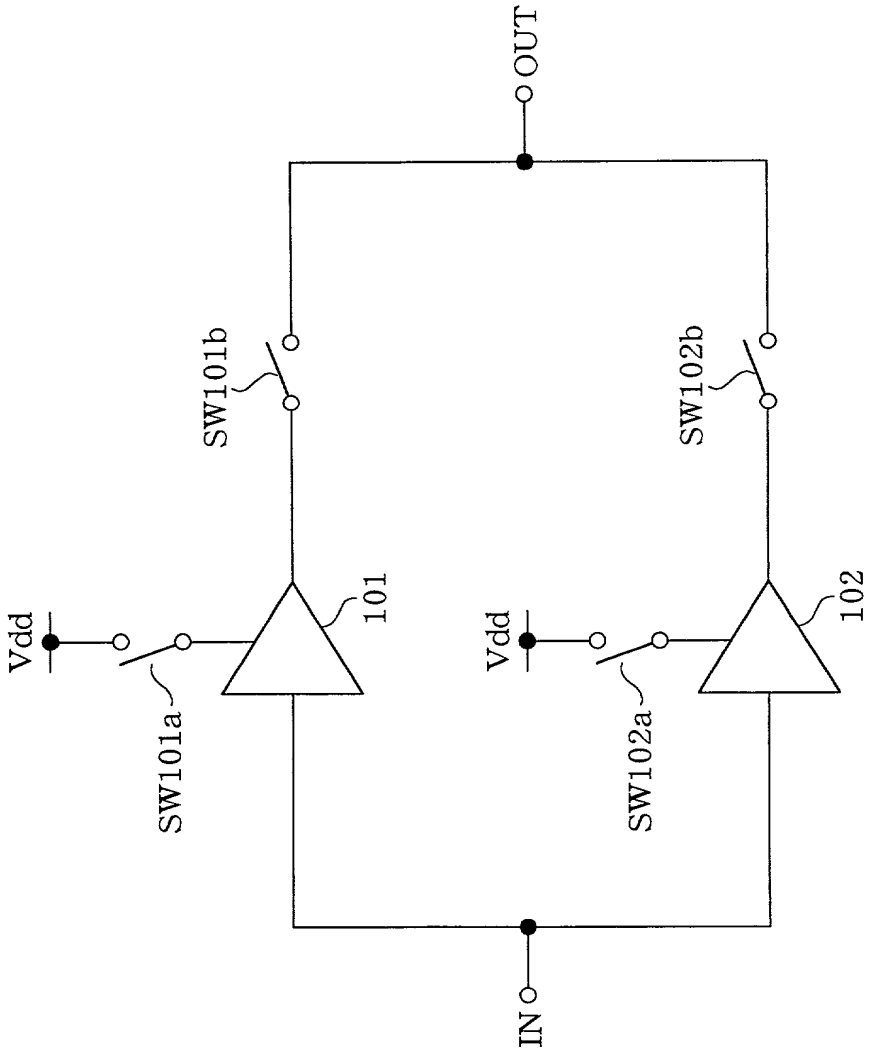


FIG. 7

FIG. 8

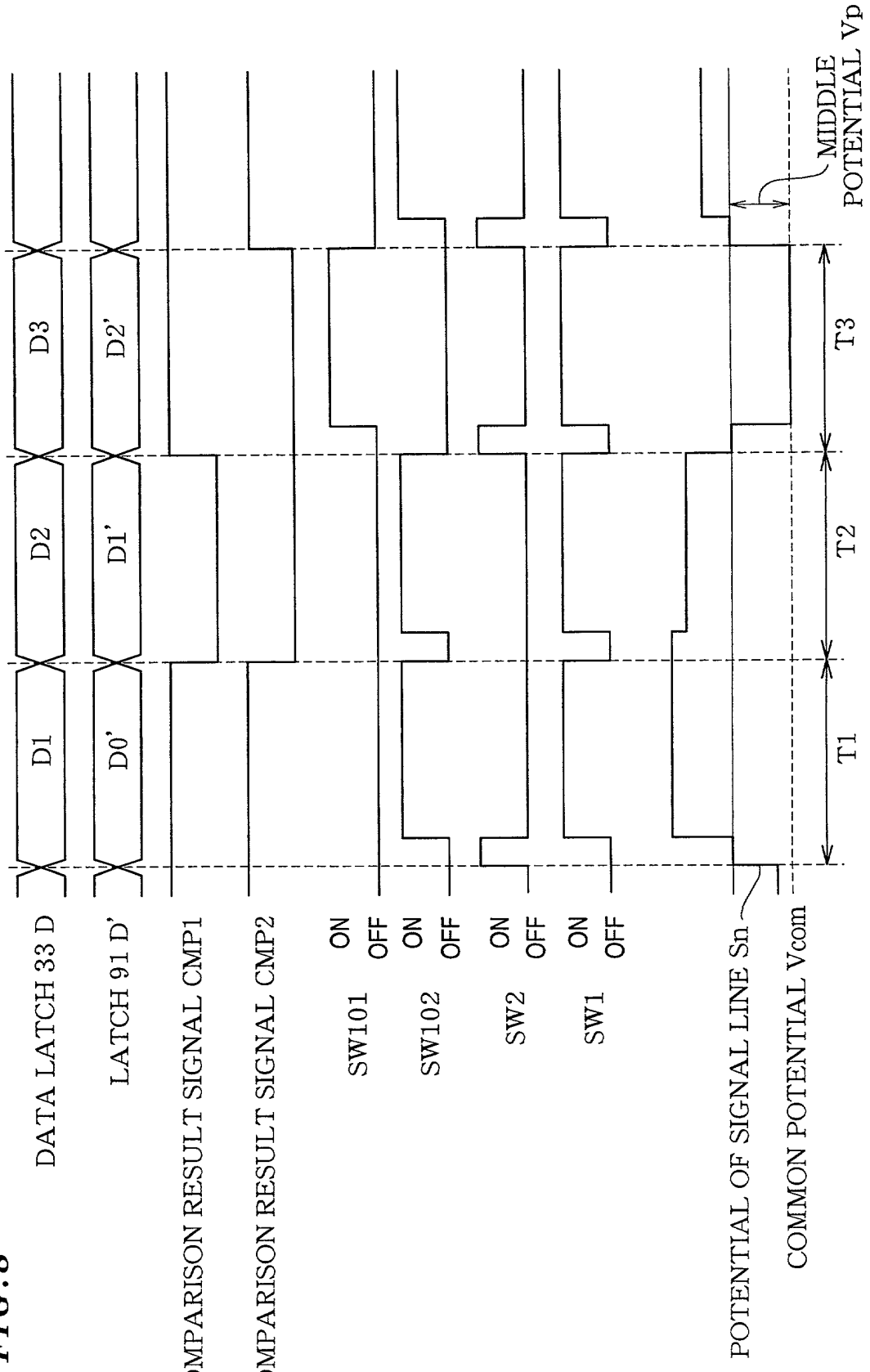

DATA LATCH 33 D
D1
D2
D3
LATCH 91 D'
D0'
D1'
D2'
COMPARISON RESULT SIGNAL CMP1
COMPARISON RESULT SIGNAL CMP2
SW101
ON
OFF
SW102
ON
OFF
SW2
ON
OFF
SW1
ON
OFF
POTENTIAL OF SIGNAL LINE Sn
COMMON POTENTIAL Vcom
MIDDLE POTENTIAL Vp
T1
T2
T3

FIG. 9

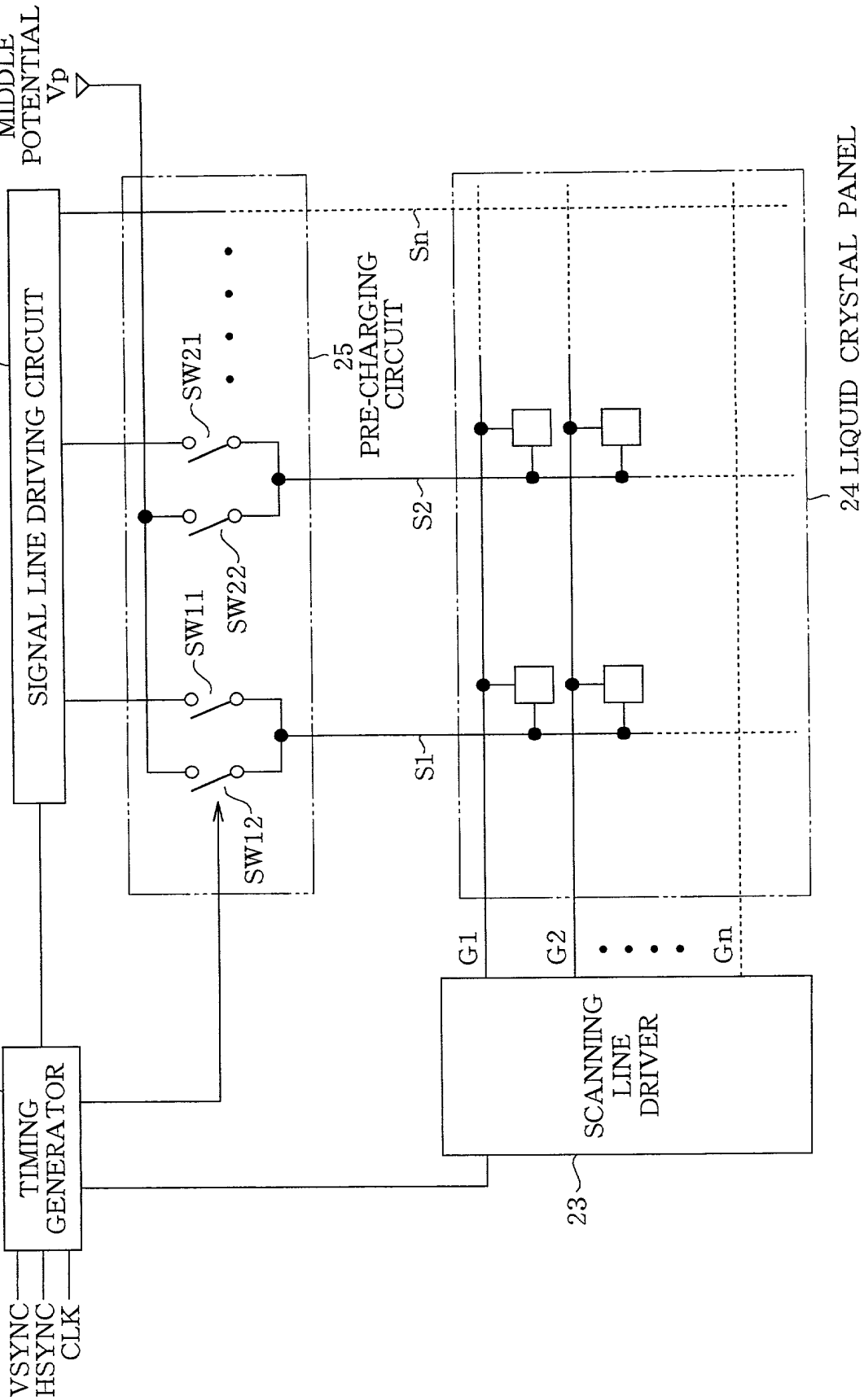

VSYNC
HSYNC
CLK
21
TIMING GENERATOR
22
SIGNAL LINE DRIVING CIRCUIT
MIDDLE POTENTIAL Vp
SW11
SW12
SW21
SW22
25
PRE-CHARGING CIRCUIT
S1
S2
Sn
24 LIQUID CRYSTAL PANEL
G1
G2
Gn
23
SCANNING LINE DRIVER

FIG. 10

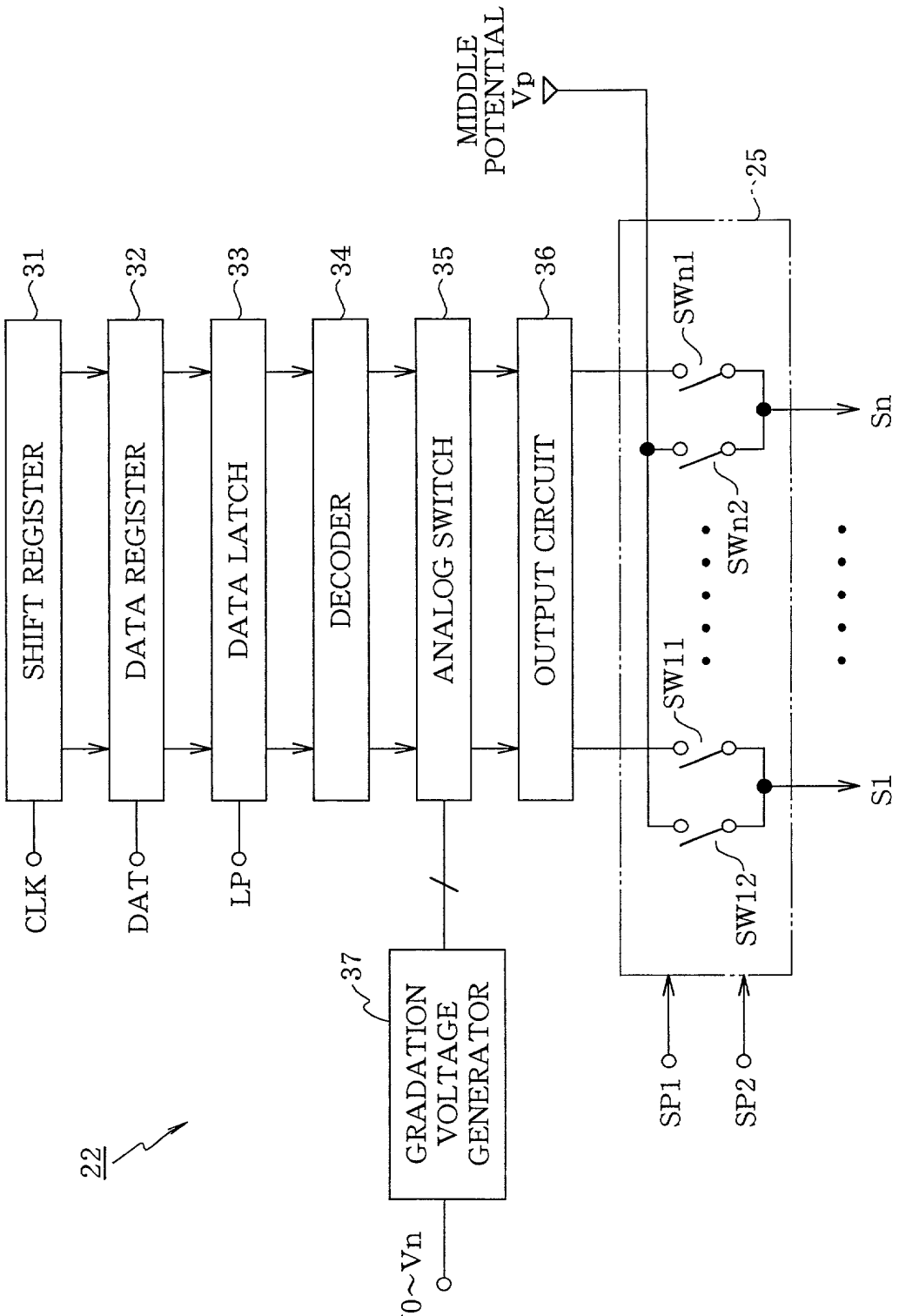
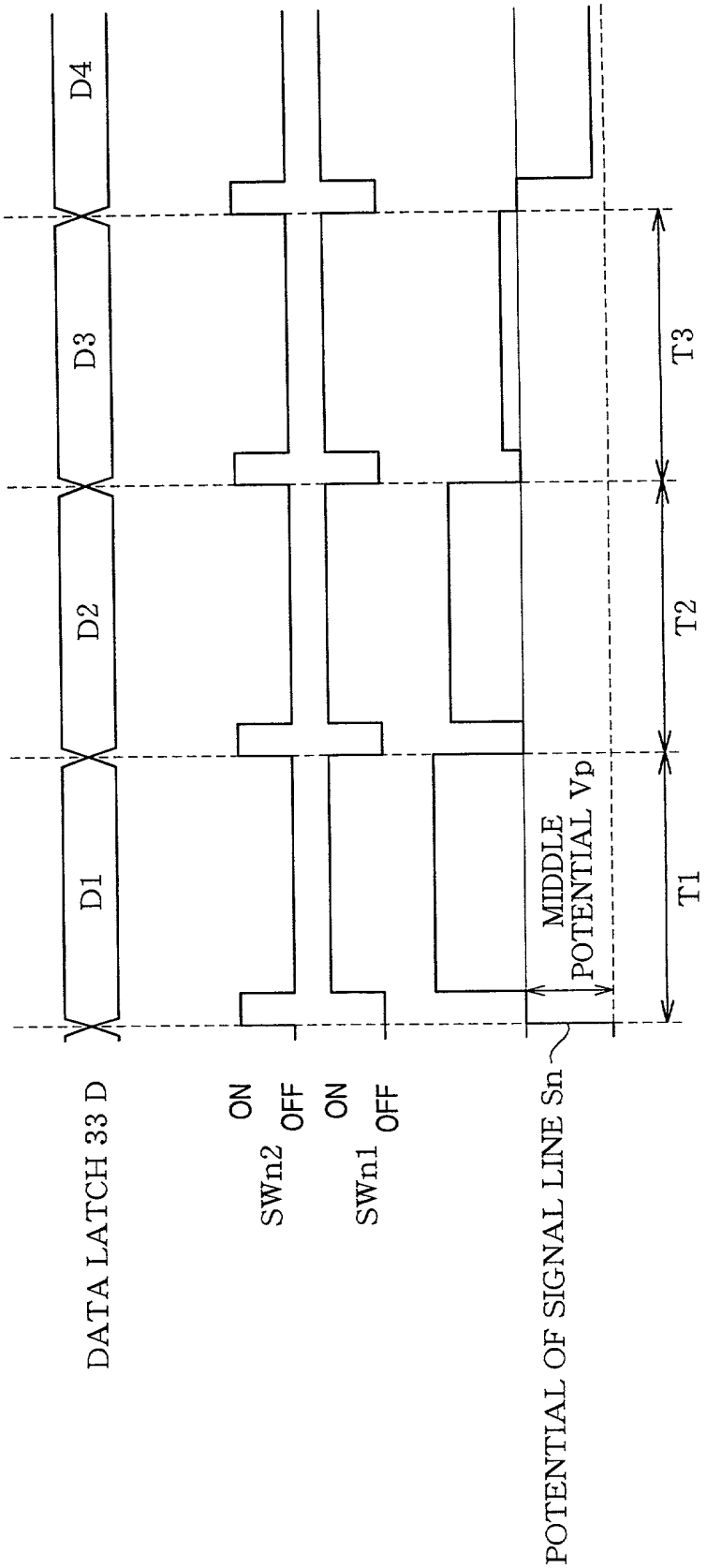

22
SHIFT REGISTER
31
DATA REGISTER
32
DATA LATCH
33
DECODER
34
ANALOG SWITCH
35
OUTPUT CIRCUIT
36
CLK
DAT
LP
GRADATION VOLTAGE GENERATOR
37
V0~Vn
MIDDLE POTENTIAL Vp
SW11
SW12
SWn1
SWn2
25
SP1
SP2
S1
Sn

FIG.11


DATA LATCH 33 D
D1
D2
D3
D4
SWn2
ON
OFF
SWn1
ON
OFF
POTENTIAL OF SIGNAL LINE Sn
MIDDLE POTENTIAL Vp
T1
T2
T3